PACE INSTITUTE OF TECHNOLOGY & SCIENCES

(Autonomous)

NH-16, Near Valluramma Temple, Ongole -523272

Accredited by NAAC with 'A' Grade and NBA

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

R21 - M.Tech (VLSI & ES) COURSE STRUCTURE

I YEAR I – SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Core - I	VLSI Technology & Design	3	0	0	3
Professional Core - II	Digital System Design	3	0	0	3
Professional Elective - I	1. CMOS Mixed Signal Circuit Design 2. VLSI Signal Processing 3. CPLD & FPGA Architectures	3	0	0	3
Professional Elective - II	1. IOT and Its Applications 2. Hardware Software Co-Design 3. Programming Languages For Embedded Systems	3	0	0	3
Lab - I	VLSI Lab	0	0	3	2
Lab - II	Digital System Design Lab	0	0	3	2
	Research Methodology & IPR	2	0	0	2
	Audit Course - I	2	0	0	0
Total Credits		**16**	**0**	**6**	**18**

I YEAR II – SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Core - III	CMOS Analog and Digital IC Design	3	0	0	3
Professional Core - IV	Real Time Operating Systems	3	0	0	3
Professional Elective - III	1. Micro Controllers For Embedded System Design 2. Network Security & Cryptography 3. Embedded Devices And Drivers	3	0	0	3
Professional Elective - IV	1. Low Power VLSI Design 2. Testing And Testability 3. SoC Design	3	0	0	3
Lab - III	CMOS Analog and Digital IC Design Lab	0	0	3	2
Lab - IV	RTOS Lab	0	0	3	2
	Mini project with Seminar	0	0	4	2
	Audit Course - II	2	0	0	0
Total Credits		**14**	**0**	**10**	**18**

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II YEAR I – SEMESTER

Course Code	Course Title	L	T	P	Credits
Professional Elective - V	1. Artificial Intelligence 2. ASIC Design 3. Parallel Processing	3	0	0	3
Open Elective	Industrial Safety Operations Research Cost Management Of Engineering Projects	3	0	0	3
Dissertation	Dissertation Phase- I (To be continued and evaluated next semester)	0	0	20	10
Total Credits					**16**

II YEAR II - SEMESTER

Course Code	Course Title	L	T	P	Credits
Dissertation	Dissertation Phase – II (Continued from III semester)	0	0	32	16
Total Credits					**16**

Audit Course I & II:

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by yoga
8. Personality Development Through Life Enlightenment Skills

Dr. R. Prakash Rao

Dr.B.Tirumala Krishna

Dr. T. Kishore Kumar

Dr. P.Rajesh Kumar

Mr. M.Teja kiran kumar

Ms. G. Mydhili

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
R21 Regulations M. Tech. (VLSI & ES) Course Structure

M.Tech. I Year I Sem **Course Structure**

L	T	P	C
3	0	0	3

VLSI TECHNOLOGY AND DESIGN

(Professional Core-1)

Internal Marks: 40
Course Code: PP21ECT01 **External Marks: 60**

Course Prerequisite: Basics of VLSI

Course Objectives:

1. To learn the basic MOS Circuits
2. To learn the MOS Process Technology
3. To understand the operation of MOS devices.
4. To understand the Layout process and standard design rules.
5. To learn the floor planning and chip design fundamentals.

Course Outcomes:

1. Understand the fabrication process of IC technology
2. Analysis of the operation of MOS transistor
3. Analysis of the physical design process of VLSI design flow
4. Able to analyzing of the design rules and layout diagram of complex problems.
5. Understand the floor planning and chip design methodologies.

UNIT-I **(10 Lectures)**

VLSI Technology: Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters.

VLSI Design: Electronic design automation concept, ASIC and FPGA design flows,SOC designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

UNIT-II **(10 Lectures)**

CMOS VLSI Design: MOS Technology and fabrication process of PMOS, NMOS, CMOS and BiCMOStechnologies, comparison of different processes.

Building Blocks of a VLSI circuit: Computer architecture, memory architectures, communication interfaces, mixedsignal interfaces.

VLSI Design Issues: Design process, design for testability, technology options, power calculations,package selection, clock mechanisms, mixed signal design.

UNIT-III **(9 Lectures)**

Basic electrical properties of MOS and BiCMOS circuits, MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitatitive and quantitative analysis with proper illustrations and necessary derivations ofexpressions.

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UNIT-IV **(9 Lectures)**

Subsystem Design and Layout: Some architectural issues switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations.

Subsystem Design Processes: Some general considerations and an illustration of design processes, design of anALU subsystem

UNIT-V **(10 Lectures)**

Floor Plan: Design Styles and specific issues, Estimating Cost of Floor plan, Slicing Structure, A Hierarchical Floor Plan.

Architecture Design: Introduction, Register-Transfer design, high-level synthesis, architectures for lowpower, architecture testing.

Chip Design: ESD Protection, Input Circuits, Output Circuits, On-chip clock Generation and Distribution, Latch-up and its prevention.

Text Books:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell,SholehEshraghian, 2005, PHI Publications.
2. Modern VLSI Design-Wayne Wolf, 3rd Ed., 1997, Pearson Education.
3. CAD for VLSI Circuits- By Experienced Faculty, JNTUK, ProfessionalPublications (2014)

Refernce Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective-Ming-BO Lin,CRC Press, 2011.
2. Principals of CMOS VLSI Design-N.H.E Weste, K. Eshraghian, 2nd Edition,Addison Wesley.

Web Reference :

1. https://nptel.ac.in/courses/117101058/
2. https://www.class-central.com/tag/vlsi%20design
3. https://www.coursera.org/learn/vlsi-cad-logic#syllabus

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M.Tech. I Year I Sem **Course Structure**

L	T	P	C
3	0	0	3

DIGITAL SYSTEM DESIGN

(Professional Core-1)

Internal Marks: 40

Course Code: PP21ECT03 **External Marks: 60**

Course Prerequisite: Digital Circuits

Course Objectives:

Students will try to learn:

1. To understand CAMP algorithms.
2. To understand characteristics of memory and their classification.
3. To understand concepts of sequential circuits and to analyze sequential systemsin terms of state machines.
4. To understand concepts of fault modeling and test pattern.
5. To implement fault detection methods.

Course Outcomes:

After successful completion of the course student will be able to

1. Develop a digital logic and apply it to solve real life problems.
2. Develop different semiconductor memories and binary arithmetic.
3. Analyze, design and implement sequential logic circuits.
4. Analyze fault detection and testing.
5. Simulate and implement fault detection methods of sequential circuits.

UNIT-I **(10 Lectures)**

Minimization Procedures and CAMP Algorithm: Review on minimization of switching functions using tabular methods, k-map, andQM algorithm

CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs, **CAMP- I algorithm,Phase-II**: Passport checking, Determination of SPC

CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II **(9 Lectures)**

PLA Design, PLA Minimization and Folding Algorithms

Introduction to PLDs, basic configurations and advantages of PLDs, PLA- Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm (IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

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UNIT –III **(9 Lectures)**

Design of Large Scale Digital Systems:

Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-IV **(10 Lectures)**

Fault Diagnosis in Combinational Circuits: Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under testmethods- Path sensitization method, Boolean difference method, properties ofBoolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT-V **(10 Lectures)**

Fault Diagnosis in Sequential Circuits: Fault detection and location in sequential circuits, circuit test approach, initial stateidentification, Haming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

Text Books:

1. Logic Design Theory-N. N. Biswas, PHI
2. Switching and Finite Automata Theory-Z. Kohavi , 2nd Edition, 2001, TMH
3. Digital system Design using PLDd-Lala

Reference Books:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – MironAbramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Son Inc.

Web Reference:

1. https://drive.google.com/file/d/1ka6HEHdCxq5hpoyK7vGTxzXfweymGfMR/view?usp=sharing
2. http://ee.sharif.edu/~asic/Lectures/Lecture_06_FPGA.pdf
3. https://drive.google.com/file/d/1DcFUopD_kou_l1P_bcna3ArG8oMAaaDs/view?usp=sharing
4. https://drive.google.com/file/d/1mhQXBP7P4p6IyGt3sKNKpKPqSiRhtsa7/view?usp=sharing
5. http://www.ece.utep.edu/courses/web5375/Notes_files/ee5375_fault_modeling.pdf

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M.Tech. I Year I Semester **Course Structure**

L	T	P	C
3	0	0	3

CMOS MIXED SIGNAL CIRCUIT DESIGN
(Professional Elective I)

Course Code: PP21ECE01 **Internal Marks:40**
Prerequisite: DSP **External marks:60**

Course Objectives:

1. Understand the basic building blocs Acquire knowledge on the large and small signal models for analog design inCMOS technology including MOSFET models,
1. Understand current Mirror and Wilson Current and Mirror circuits
2. Acquire knowledge on amplifiers (single-/multi-stage, differential and operational) in CMOS technology,
3. Understand the different logic circuit designs for logic expressions and theimportance of the circuit designs,
4. Understand the designs both in combinational as well as sequential.

Course Outcomes:

The Students at the end of the course must be able to:

1. Describe the large and small signal models for analog design in CMOS technology including MOSFET models.
2. Analyze current mirrors and voltage references taking supply, temperatureand process variations into account.
3. Analyze amplifiers (single-/multi-stage, differential and operational) in CMOStechnology.
4. Realize the different logic circuit designs for logic expressions and the importance of the circuit designs.
5. Understand the designs both in combinational as well as sequential.

UNIT-I

Switched Capacitor Circuits Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integratorsfirst order filters, Switch sharing, biquad filters.

UNIT-II

Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detectorand charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III

Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters,Hybrid converters

UNIT-IV

Nyquist Rate A/D Converters Successive approximation converters,Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT-V

Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXTBOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMHEdition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg,
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, WileyStudent Edition, 2013

REFERENCEBOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, WileyInterscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009.

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M.Tech. I Year I Semester **Course Structure**

L	T	P	C
3	0	0	3

VLSI SIGNAL PROCESSING
(Professional Elective –I)

Internal Marks: 40

Course Code: PP21**E**C**E0**2 **External Marks: 60**

Course Prerequisite: DSP

Course Objectives:

1. Introduce students to the fundamentals of VLSI signal processing and exposethem to examples of applications.
2. Design and optimize VLSI architectures for basic DSP algorithms.
3. To make an in depth study of DSP structures amenable to VLSIimplementation.
4. To enable students to design VLSI system with high speed and low power.
5. To introduce techniques for altering the existing DSP structures to suit VLSIimplementations.
6. To introduce efficient design of DSP architectures suitable for VLSI

Course Outcomes:

1. Understand VLSI design methodology for signal processing systems.
2. Familiar with VLSI algorithms and architectures for DSP.
3. Able to implement basic architectures for DSP using CAD tools.
4. Ability to modify the existing or new DSP architectures suitable for VLSI.
5. Be able to make use of Transformation Techniques.

Unit I **(10 Lectures)**

Introduction To DSP Systems:

Introduction; representation of DSP algorithms: Block Diagram, signal flow graph, data flow graph, dependence graph. Iteration Bound: Data flow graph representations, loop bound and iteration bound, longest path matrix algorithm, iteration bound of Multirate data flow graphs.

Unit II **(10 Lectures)**

Pipelining and Parallel Processing:

Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.

Unit III **(10 Lectures)**

Unfolding: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in MultirateSystems.

Unit IV **(9 Lectures)**

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

Unit V **(9 Lectures)**

Fast Convolution:

Introduction, Cook, Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

Textbooks:

1. Keshab K. Parhi. VLSI Digital Signal Processing Systems, Wiley-InterSciences, 1999
2. Mohammed Ismail, Terri, Fiez, Analog VLSI Signal and Information Processing, McGraw Hill, 1994.
3. Kung. S.Y., H.J. While house T.Kailath, VLSI and Modern singalprocessing, Prentice Hall, 1985.

References:

1. Jose E. France, YannisTsividls, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing' Prentice Hall, 1994.
2. Keshab k. Parhi," VLSI Digital Signal Processing Systems: Design and Implementation", Wiley, inter science. REFERENCE BOOKS 1.S.Y.kung, H.J.White house, T. Kailath," VLSI and Modern Signal Processing", Prentice hall,

Web Reference:

1. http://www.ece.ucdavis.edu/~bbaas/281/notes/Lecture01.pdf\
2. https://drive.google.com/file/d/0BzoKWH8M1BoTb1d4SVNFSlZMdHM/view
3. https://drive.google.com/file/d/0BzoKWH8M1BoTdUpldzR3QkY3QlU/v iew

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M.Tech. I Year I Semester **Course Structure**

L	T	P	C
3	0	0	3

CPLD & FPGA ARCHITECTURES

(Professional Elective -I)

Internal Marks: 40

Course Code: PP21**E**C**E0**3 **External Marks: 60**

Course Prerequisite: VLSI Design

Course Objectives:

1. Gain a knowledge on different PLD's, CPLD architectures.
2. Gain knowledge on different FPGA architectures and it CLB's.
3. Gain knowledge on SRAM programming technologies of FPGA's.
4. Get an idea on Anti-Fuse Programming technologies of FPGAs
5. Get the practical knowledge of working on a a back end tool ,implementingsome designs using tools

Course Outcomes:

On successful completion of this course the

1. Student can understand the concepts of CPLD's and their architectures.
2. Student can understand the concepts of FPGA's and their architectures.
3. Student can perform the SRAM based programming for FPGA's.
4. Student can perform the Antifuse based programming for FPGA's.
5. Student can apply appropriate techniques, Resources and tools in, Modelingcomplex engineering applications with an understanding of limitations.

UNIT-I **(10 Lectures)**

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II **(10 Lectures)**

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

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UNIT –III **(10 Lectures)**

SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT –IV **(9 Lectures)**

Anti-Fuse Programmed FPGAs:

Introduction, Programming Technology, Device Architecture, The Actel ACT1,ACT2 and ACT3 Architectures.

UNIT –V **(9 Lectures)**

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, CengageLearning

Reference Books:

1. P.K.Chan & S. Mourad, “Digital Design Using Field Programmable Gate Array”,jPrentice Hall (Pte), 1994.
2. S.Trimberger, Edr., “Field Programmable Gate Array Technology”, KluwerAcademic Publicatgions, 1994.
3. J. Old Field, R.Dorf, “Field Programmable Gate Arrays”, John Wiley & Sons,Newyork, 1995. 4. S.Brown, R.Francis, J.Rose, Z.

Web Reference:

1. https://www.researchgate.net/.../3250064_FPGA_and_CPLD_architectures_a_tut orial
2. https://www.slideshare.net/sudhirshelke73/unit-vi-cpldfpga-architecture
3. https://www.scribd.com/doc/24072222/m-tech-Cpld-Fpga-Architecture- Applications

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M.Tech. I Year I Semester **Course Structure**

L	T	P	C
3	0	0	3

IoT & Its APPLICATIONS

(Professional Elective –II)

Internal Marks: 40

Course Code: PP21ECE04 **External Marks: 60**

Course Prerequisite: Python Programming

Course Objectives:

1. To introduce the Iot terminology, technology and its applications
2. To introduce the raspberry PI platform, that is widely used in IoT applications
3. To introduce the implementation of web based services on IoT devices

Course Outcomes:

1. Understand the new computing technologies
2. Ability to introduce the concept of M2M (machine to machine) with necessaryprotocols
3. Able to apply the latest computing technologies like cloud computing technologyand Big Data
4. Get the skill to program using python scripting language which is used in manyIoT devices

UNIT- I **(10 Lectures)**

Introduction to Internet of Things –Definition and Characteristics of IoT, Physical Design of IoT – IoT Protocols, IoT Communication Models, Iot Communication APIs, IoT enabaled Technologies – Wireless Sensor Networks, Cloud Computing, Big data analytics, Communication protocols, Embedded Systems.

UNIT -II **(9 Lectures)**

IoT and M2M – Software defined networks, network function virtualization, difference between SDN and NFV for IoT, Basics of IoT System Management with NETCOZF, YANGNETCONF, YANG, SNMP NETOPEER

UNIT- III **(10 Lectures)**

IoT Programming and interfacing - Introduction to Python - Language features of Python, Introduction to Raspberry PI-Interfaces (serial, SPI, I2C) Programming – Python program with Raspberry PI with focus of interfacing external gadgets, controlling output and reading input from pins.

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UNIT- IV **(10 Lectures)**

IoT Physical Servers and Cloud Offerings – Introduction to Cloud Storage models and communication APIs Webserver – Web server for IoT, Cloud for IoT, Python web application framework Designing a RESTful web API

UNIT-V **(9 Lectures)**

Case Study & advanced IoT Applications- IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT.

Text Books:

1. Internet of Things - A Hands-on Approach, Arshdeep Bahga and VijayMadisetti, Universities Press, 2015,
2. Getting Started with Raspberry Pi, Matt Richardson & Shawn Wallace, O'Reilly(SPD), 2014

References Books:

1. Peter Waher, “Learning Internet of Things”, PACKT publishing,BIRMINGHAM – MUMBAI
2. The Internet of Things, by Michael Millen, Pearson

Web Reference :

1. https://www.coursera.org/specializations/iot
2. https://www.tutorialspoint.com/internet_of_things/internet_of_things_tutorial
3. https://www.mmh.com/topic/category/iot
4. cseweb.ucsd.edu/classes/wi15/cse237A-a/handouts/8_iot.pdf

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M.Tech. I Year I Semester **Course Structure**

L	T	P	C
3	0	0	3

HARDWARE SOFTWARE CO-DESIGN

(Professional Elective -II)

Internal Marks: 40

Course Code: PP21ECE05 **External Marks: 60**

Course Prerequisite: Embedded Systems

Course Objectives:

1. To do hardware/software co-design for embedded systems.
2. To develop skills in analysis, approach, optimization, and implementationof embedded systems.
3. To exploiting the synergism of hardware and software through their concurrent design.
4. To Develop High-Level Hardware Synthesis Capabilities
5. The Importance Of Codesign Improves Design Quality, Design Cycle Time,And Cost.

Course Outcomes:

Upon the completion of the course student will be able to

1. Understand architectural languages and co-synthesis algorithms for co-design.
2. Understand prototyping and emulation systems and target architectures.
3. Apply compilation tools and techniques for embedded processor architectures.
4. will be able to analysis, design and testing of systems that include both hardware and software.
5. will be able to estimate if additional hardware can accelerate a system.

UNIT –I **(9 Lectures)**

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioningdistributed system co-synthesis.

UNIT –II **(11 Lectures)**

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and mulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), and Mixed Systems.

UNIT –III **(8 Lectures)**

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV **(10 Lectures)**

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V **(10 Lectures)**

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis,system level specification languages,
Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi language co-simulation, the cosymasystem and lycos system.

Text Books:

1. Jorgen Staunstrup, Wayne Wolf, "Hardware / Software Co- Design Principlesand Practice", 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, "Hardware / Software Co-Design", 2002, Kluwer Academic Publishers

Reference Books:

1. Patrick R.Schaumont, "A Practical Introduction to Hardware/SoftwareCo- design", 2010, Springer
2. Jean-Michel Berge (1997), "Hardware/Software Co-Design and Co-Verification", Kluwer Publications.

Web Reference:

1. https://pdfs.semanticscholar.org/presentation
2. http://rijndael.ece.vt.edu/gezel2/book.html
3. https://www.sciencedirect.com/science/book
4. https://dl.acm.org/citation.cfm
5. https://www.kobo.com/us/en/ebook/a-practical-introduction-to-hardware-software-codesign

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

M.Tech. I Year I Semester **Course Structure**

L	T	P	C
3	0	0	3

PROGRAMMING LANGUAGES FOR EMBEDDED SYSTEMS

(Professional Elective II)

Internal Marks: 40

Course Code: PP21ECE06 **External Marks: 60**

Course Prerequisite: C-Language

Course Outcomes:

At the end of this course, students will be able to
1. Write an embedded C application of moderate complexity.
2. Develop and analyze algorithms in C++.
3. Differentiate interpreted languages from compiled languages.

Unit 1

Embedded „C" Programming Bitwise operations, Dynamic memory allocation, OS services. Linked stack and queue, Sparse matrices, Binary tree. Interrupt handling in C, Code optimization issues. Embedded Software Development Cycle and Methods (Waterfall, Agile)

Unit 2

Object Oriented Programming Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

Unit 3

CPP Programming: „cin", „cout", formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, „this" pointer, constructors, destructors, friend function, dynamic memory allocation

Unit 4

Overloading and Inheritance: Need of operator overloading, overloading the assignment, Overloading using friends, type conversions, single inheritance, base and derived classes, friend Classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, Polymorphism, virtual functions.

Unit 5

Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions.
Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

Text Books:

1. Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, "Learning Perl", O"Reilly Publications, 6th Edition 2011

Reference Books:

1. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002
2. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
3. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey & Sons, 2005Kaufmann.

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M.Tech. I Year I Semester **Course Structure**

L	T	P	C
0	0	3	2

VLSI LABORATORY

Internal Marks: 40

Course Code: PP21ECL01 **External Marks: 60**

Course Objectives:

1. To learn VHDL for modeling of combinational and sequential circuits.
2. To know the Verification and functionality of designed circuits using functional simulators.
3. To learn the Synthesis procedure of designed circuits.
4. To learn the Implementation of designed circuits using various FPGA kits.

Course Outcomes:

After going through this course the student will be able to

1. Can get the knowledge to implement the digital design on FPGA.
2. Synthesize the encoding techniques by using the Xilinx ISE Simulator.
3. Simulate combinational and sequential circuits using CAD tools.
4. Design digital systems that are reconfigurable for testing and test it on FPGA

Any 10 of The Following Experiments are to be conducted:

PROGRAMS:

1. Parity Encoder.
2. Random Counter
3. Single Port Synchronous RAM.
4. Synchronous FIFO.
5. ALU.
6. UART Model.
7. Dual Port Asynchronous RAM.
8. Fire Detection and Control System using Combinational Logic circuits.
9. Traffic Light Controller using Sequential Logic circuits
10. Pattern Detection using Moore Machine.
11. Finite State Machine (FSM) based logic circuit.
12. Design of 4 bit Multiply and Accumulate unit.

Lab Requirements:

Software:

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Perl Software.

Hardware:

Personal Computer with necessary peripherals, configuration and operating Systemand relevant VLSI (CPLD/FPGA) hardware Kits.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

M.Tech. I Year I Semester **Course Structure**

L	T	P	C
0	0	3	2

DIGITAL SYSTEM DESIGN LAB

Internal Marks: 40

Course Code: PP21ECL03 **External Marks: 60**

Pre Requisite:

Systems Design experiments:

- The students are required to design the logic to perform the following experiments using necessary Industry standard simulator to verify the logical /functional operation, perform the analysis with appropriate synthesizer and to verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).
- Consider the suitable switching function and data to implement the required logic if required.

A student has to do at least 10 Experiments.

List of Experiments:

1. Determination of EPCs using CAMP-I Algorithm.
2. Determination of SPCs using CAMP-I Algorithm.
3. Determination of SCs using CAMP-II Algorithm.
4. PLA minimization algorithm (IISc algorithm)
5. PLA folding algorithm(COMPACT algorithm)
6. ROM design.
7. Control unit and data processor logic design
8. Digital system design using FPGA.
9. Kohavi algorithm.
10. Hamming experiments.

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M.Tech. I Year I Semester **Course Structure**

L	T	P	C
2	0	0	2

RESEARCH METHODOLOGY AND IPR

Internal Marks: -

Course Code: PP21MCT01 **External Marks: -**

Course Prerequisites: Nil

Course Objectives:

1. understand some basic concepts of research and its methodologies
2. identify appropriate research topics
3. select and define appropriate research problem and parameters
4. prepare a project proposal (to undertake a project)
5. organize and conduct research (advanced project) in a more appropriatemanner.
6. The main objective of the IPR is to make the students aware of their rights forthe protection of their invention done in their project work.

Course Outcomes:

At the end of this course, students will be able to

1. Understand research problem formulation.
2. Analyze research related information
3. Follow research ethics
4. Understand that today's world is controlled by Computer, InformationTechnology, but tomorrow world will be ruled by ideas, concept, and creativity.
5. Understanding that when IPR would take such important place in growth ofindividuals & nation, it is needless to emphasis the need of information aboutIntellectual Property Right to be promoted among students in general & engineering in particular.
6. Understand that IPR protection provides an incentive to inventors for furtherresearch work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT- I **(4 Lectures)**

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scopen and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis,interpretation, Necessary instrumentations.

UNIT-II **(4 Lectures)**

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Formatof research proposal, a presentation and assessment by a review committee.

UNIT-III **(4 Lectures)**

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting,development.
International Scenario: International cooperation on IntellectualProperty. Procedure for grants of patents, Patenting under PCT.

UNIT-IV **(4 Lectures)**

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology.Patent information and databases. Geographical Indications.

UNIT-V **(4 Lectures)**

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledgeCase Studies, IPR and IITs.

Text Books:

1. Stuart Melville and Wayne Goddard, "Research methodology: anintroduction for science & engineering students'
2. Wayne Goddard and Stuart Melville, "Research Methodology: AnIntroduction
3. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand,2008

References Books:

1. Ranjit Kumar, 2 ndEdition, "Research Methodology: A Step by StepGuide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " IntellectualProperty in NewTechnological Age", 2016.

Web Reference :

1. https://www.isical.ac.in/~palash/research-methodology/RM-lec4.pdf\
2. http://www.bitspilani.ac.in/uploads/Patent_ManualOct_25th_07.pdf
3. https://my.cumbria.ac.uk/media/MyCumbria/IPR-notes-and-guidance.pdf

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M.Tech. I Year I Semester **Course Structure**

L	T	P	C
2	0	0	0

ENGLISH FOR RESEARCH PAPER WRITING
(Audit-I)

Internal Marks: 100

Course code:PP21ECA01: **External Marks: -**

Course Prerequisite: Nil

Course Objectives:

Students will be able to:

1. Understand that how to improve your writing skills and level of readability
2. Learn about what to write in each section
3. Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission.

UNIT-I **(4 Lectures)**

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, AvoidingAmbiguity and Vagueness.

UNIT-II **(4 Lectures)**

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising,Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction.

UNIT-III **(4 Lectures)**

Review of the Literature, Methods, Results, Discussion, Conclusions, The FinalCheck.

UNIT-IV **(4 Lectures)**

key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT-V **(4 Lectures)**

skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be thefirst- time submission.

References Books:

1. Goldbort R (2006) Writing for Science, Yale University Press (available onGoogle Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge UniversityPress
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM.Highman's book .
4. Adrian Wallwork , English for Writing Research Papers, Springer New YorkDordrecht Heidelberg London, 2011

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M.Tech. I Year I Semester **Course Structure**

L	T	P	C
3	0	0	3

CMOS ANALOG AND DIGITAL IC DESIGN

(Professional Core-III)

Internal Marks: 40

Course Code: PP21ECT02 **External Marks: 60**

Course Prerequisite: STLD& IC Design

Course Objectives:

1. Acquire knowledge on the large and small signal models for analog design inCMOS technology including MOSFET models,
2. Understand current Mirror and Wilson Current Mirror circuits
3. Acquire knowledge on amplifiers (single-/multi-stage, differential and operational) in CMOS technology,
4. Understand the different logic circuit designs for logic expressions and theimportance of the circuit designs,
5. Understand the designs both in combinational as well as sequential.

Course Outcomes:

The Students at the end of the course must be able to:

1. Describe the large and small signal models for analog design in CMOStechnology including MOSFET models.
2. Analyze current mirrors and voltage references taking supply, temperatureand process variations into account.
3. Analyze amplifiers (single-/multi-stage, differential and operational) in CMOStechnology.
4. Realize the different logic circuit designs for logic expressions and theimportance of the circuit designs.
5. Understand the designs both in combinational as well as sequential.

UNIT –I **(9 Lectures)**

MOS Devices and Modeling: The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT –II **(10 Lectures)**

Analog CMOS Sub-Circuits:

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-

Current mirror with Beta Helper, Degeneration, Cascade current

Mirror and Wilson Current Mirror, Current and Voltage References, Band gapReference.

CMOS Amplifiers:

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures. Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps.

UNIT-III **(9 Lectures)**

MOS Design:

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-IV **(10 Lectures)**

Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design.CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

Sequential MOS Logic Circuits:

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-V **(10 Lectures)**

Dynamic Logic Circuits:

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Text Books:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg,Oxford University Press, International Second Edition/Indian Edition,2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, PaulJ. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.
3. Digital Integrated Circuit Design – Ken Martin, Oxford University Press,2011.
4. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, WileyStudentEdn, 2013.
2. Introduction to VLSI Systems: A Logic, Circuit and System Perspective –Ming-BO Lin, CRC Press, 2011

Web Reference:

1. https://books.google.co.in/books?isbn=0199937427
2. https://books.google.co.in/books?isbn=047137752X
3. https://books.google.co.in/books?isbn=0195125843
4. https://books.google.co.in/books?isbn=0070530777
5. https://books.google.co.in/books?isbn=8126517786

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

M.Tech. I Year I Semester **Course Structure**

L	T	P	C
3	0	0	3

REAL TIME OPERATING SYSTEMS

(Professional Core-IV)

Internal Marks: 40

Course Code: PP21ECT04 **External Marks: 60**

Course Prerequisite: OS, Embedded System

Course Objective:

To learn

1. Basic concepts Operating Systems
2. Real-time systems and Real-time Operating Systems
3. Design and analysis of computer systems for real-time applications.
4. Resource management, time-constrained communication
5. Initiate research in Real Time Systems
6. Scheduling and imprecise computations, real-time kernels.

Course Outcome:

On completion of the course, students will be knowledgeable in

1. Real-time embedded systems
2. Real time operating system concepts
3. various real-time operating systems.
4. Identifying variable faults in Embedded systems.
5. Commercial RTOS
6. Real time system reference model
7. Real time scheduling approaches

UNIT I **(10 Lectures)**

Review Of Operating Systems:

Basic Principles - Operating System structures – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes–Introductionto Distributedoperatingsystem– Distributed scheduling.

UNIT II **(10 Lectures)**

Overview Of RTOS:

RTOS Task and Task state - Process Synchronization- Message queues – Mail boxes - pipes – Critical section – Semaphores – Classical synchronization problem –Deadlocks

UNIT III **(11 Lectures)**

Real Time Models And Languages:

Event Based – Process Based and Graph based Models – Real Time Languages –RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT IV **(9 Lectures)**

Real Time Kernel:

Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target– Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

UNIT V **(8 Lectures)**

RTOS Application Domains:

RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for faultTolerant Applications – RTOS for Control Systems.

Text Books:

1. Raj Kamal, "Embedded Systems- Architecture, Programming and Design"Tata McGraw Hill, 2006.
2. Herma K., "Real Time Systems – Design for distributed EmbeddedApplications", Kluwer Academic, 1997
3. C.M. Krishna, Kang, G.Shin, "Real Time Systems", McGraw Hill, 1997.

References:

1. Charles Crowley,"Operating Systems-ADesign Oriented approach", McGrawHill 1997.
2. Raymond J.A.Bhur, Donald L.Bailey, "An Introduction to Real Time Systems",PHI 1999.
3. Mukesh Sighal and N. G. Shi "Advanced Concepts in Operating System",McGraw Hill 2000.

Web Reference :

1. https://cseweb.ucsd.edu/classes/wi13/cse237A-a/handouts/rtos-chap11.pdf
2. http://chettinadtech.ac.in/g_articlen/10-06-28/10-06-28-08-23-52-pratheesh.pdf
3. http://real-time operating systems the engineering of real-time embeddedsystems book 1
4. real-time embedded components and systems with linux and rtos engineering
5. real-time concepts for embedded systems.
6. real-time systems design principles for distributed embedded applications real-time systems series.

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M.Tech. I Year II Sem **Course Structure**

L	T	P	C
3	0	0	3

MICRO CONTROLLERS FOR EMBEDDED SYSTEM DESIGN

(Professional Elective-III)

Internal Marks: 40

Course Code: PP21ECE07 **External Marks:** 60

Course Prerequisite: Micro Processors and advanced Micro controllers

Course Objectives:

1. To understand the design aspects of ARM processors.
2. Basic introduction for programming on ARM processor
3. Able to understand C programming using for ARM processor
4. To describe various cache-technologies that surrounds the ARM cores.

Course Outcomes:

Upon completion of the course students will be able to

1. Understand and analyze the design aspects, Architecture, and instruction setassociated with ARM processors.
2. Analyze the C programming optimization methods for ARM processor
3. Examines various cache-technologies that surround the ARM cores.

UNIT-I **(9 Lectures)**

ARM Architecture - ARM Design Philosophy, Registers, PSR, Pipeline, Interruptsand Vector Table, Architecture Revision, ARM Processor Families.

UNIT II **(10 Lectures)**

ARM Programming Model-I - Instruction Set: Data Processing Instructions, Branch,Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT III **(10 Lectures)**

ARM Programming Model-II - Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load- Store Instructions, Stack, Software Interrupt Instructions

UNIT IV **(10 Lectures)**

ARM Programming - Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT V **(9 Lectures)**

Memory Management - Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Content Switch.

Text Books:

1. Andrew Sloss, Dominic Symes, Chris Wright, "ARM system Developers Guide: Designing and Optimizing System Software", Elsevier publications, 2004.

Reference Books:

1. Valvano, J. (2011),"Embedded microcomputer systems: real time interfacing", 3rd Edition, Cengage Learning.

Web Reference:

1. https://www.arm.com/products/processors
2.https://developer.arm.com/products/architecture/cpu-architecture
3.https://en.wikipedia.org/wiki/ARM_architecture
4.https://www.cs.ccu.edu.tw/~pahsiung/courses/ese/.../ESD_03_ARM_Architecture.pdf

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M.Tech. I Year II Semester **Course Structure**

L	T	P	C
3	0	0	3

NETWORK SECURITY AND CRYPTOGRAPHY

(Professional Elective-III)

Internal Marks: 40

Course Code: PP21ECE08 **External Marks: 60**

Course Prerequisite: Fundamental of Computer Protocols

Course Objectives:

1. To understand the fundamentals of computer security.
2. To comprehend and apply authentication services, authentication algorithms.
3. To analyze asymmetric ciphers.
4. To understand the conventional methods of cyber security.
5. To understand the conventional methods of IP security.

Course Outcomes:

1. Interpreting the OSI standard with the layered architecture to provide networksecurity.
2. Building of encryption standards for protecting the networks.
3. Evaluate security mechanisms using rigorous approaches, theoretically.
4. Design a security solution for a given application with respect to cyber security.
5. Ability to protect the current legal issues provide the desired IP security.

Unit I **(8 Lectures)**

Computer security concepts, OSI security Architecture, Security attacks, Security Services, Security mechanisms, A model for network security.

Unit II **(10 Lectures)**

Encryption Standards: Classical Encryption Techniques, Symmetric Cipher Model ,Substitution Techniques, Transposition Techniques ,Rotor Machines, Steganography

Block Cipher Principles: Stream Ciphers and Block Ciphers, Motivation for the Feistel Cipher Structure, The Feistel Cipher, The Data Encryption Standard: DES Encryption, DES Decryption.

Unit III **(10 Lectures)**

Asymmetric ciphers : Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, ElGamal cryptosystem, Elliptic Curve Arthimatic, Elliptic Curve Cryptograpy.Number Theory: Prime numbers, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Unit-IV **(9 Lectures)**

Cyber security Overview: Security from a global perspectives, Trends and types of attacks and malware, The tpes of malwares, Network and Information InfrastructureDefense overview.

Unit-V **(11 Lectures)**

IP Security Overview: Applications of Ipsec, Benefits of Ipsec, Routing Applications, IPsec Documents IPsec Services ,Transport and Tunnel Modes. IP Security Policy: Security Associations, Security Association Database, SecurityPolicy Database, IP Traffic Processing.

Encapsulating Security Payload: ESP Format, Encryption and Authentication Algorithms, Padding, Anti-Replay Service, Transport and Tunnel Modes

Textbooks:

1. Cryptography & Network Security: Principles and Practices, William Stallings,PEA, Fifth edition
2. Introduction to Computer Networks & Cyber Security, Chwan Hwa Wu,J.David Irwin, CRC press.

References Books:

1. V k Pachghare: Cryptography and Information Security, PHE ,2013.
2. Aaron E. Earle, “Wireless Security Handbook”, Auerbach publications, Taylor& Francis Group, 2006.
3. Yang Xiao and Yi Pan, “Security in Distributed and NetworkingSystems”, World Scientific, 2007, Chapter 1.

Web Reference:

1. https://nptel.ac.in/syllabus/106105031/
2. www.cse-web.iitkgp.ernet.in/~debdeep/courses_iitkgp/Crypto/index.html

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M.Tech. I Year II Semester **Course Structure**

L	T	P	C
3	0	0	3

EMBEDDED DEVICE DRIVERS

(Professional Elective –III)

Internal Marks: 40

Course Code: PP21ECE09 **External Marks: 60**

Course Prerequisite: Micro Processors and Micro Controllers

Course Objectives: ·

1. To know about the Device Drivers need and loadable modules
2. To Learn the debugging techniques and Advanced char driver operations
3. To Learn the Concurrency and Race Conditions
4. To Understand fundamentals of hardware interface with kernel
5. To acquire knowledge on interrupt handling and kernel data types

Course Outcomes:

Upon the completion of this course students will be able to:

1. Understands the Device Drivers need and loadable modules
2. Learn the debugging techniques and Advanced char driver operations
3. Understand Concurrency and Race Conditions
4. Understand fundamentals of hardware interface with kernel
5. Use and get acquaint to interrupt handling and kernel data types

UNIT-I **(10 Lectures)**

An Introduction to Device Drivers: The Role of the Device Driver, Splitting the Kernel, Classes of Devices and Modules,Security Issues, Version Numbering

Building and Running Modules: Setting Up Your Test System, The Hello World Module, Kernel Modules Versus Applications, Compiling and Loading, The Kernel Symbol Table, Preliminaries, Initialization and Shutdown, Module Parameters, Doing It in User Space

UNIT-II **(10 Lectures)**

Char Drivers: The Design of scull, Major and Minor Numbers, Some Important Data Structures, Char Device Registration, open and release, scull's Memory Usage, read and write, Playing with the New Devices.

Debugging Techniques: Debugging Support in the Kernel, Debugging by Printing, Debugging by Querying, Debugging by Watching, Debugging System Faults, Debuggers and Related Tools.

UNIT-III **(10 Lectures)**

Concurrency and Race Conditions:

Pitfalls in scull, Concurrency and Its Management, Semaphores and Mutexes, Completions, Spinlocks, Locking Traps, Alternatives to Locking

Advanced Char Driver Operations:

Octl, Blocking I/O, poll and select, Asynchronous Notification, Seeking a Device, Access Control on a Device File.

UNIT-IV **(9 Lectures)**

Time, Delays, and Deferred Work:

Measuring Time Lapses, Knowing the Current Time, Delaying Execution, Kernel Timers, Tasklets, Work queues

Allocating Memory:

The Real Story of kmalloc, Look aside Caches, get_free_page and Friends, vmalloc and Friends, Per-CPU Variables, Obtaining Large Buffers **Communicating with Hardware** - I/O Ports and I/O Memory, Using I/O Ports, An I/O Port Example, Using I/O Memory.

UNIT-V **(9 Lectures)**

Interrupt Handling:

Preparing the Parallel Port, Installing an Interrupt Handler, Implementing aHandler, Top and Bottom Halves, Interrupt Sharing, Interrupt-Driven I/O

Data Types in the Kernel:

Use of Standard C Types, Assigning an Explicit Size to Data Items, Interface-Specific Types, Other Portability Issues, Linked Lists.

Text Books:

1. Jonathan Corbet, Alessandro Rubini, and Greg Kroah-Hartman (2005), "LinuxDevice Drivers" O'Reilly Third Edition

Reference Books:

1. Robert Love, "Linux Kernel Development", 3rd Edition, Addison-WesleyProfessiona.
2. Sreekrishnan Venkateswaran, "Essential Linux Device Drivers", Prentice Hall

Web Reference :

1. https://www.coursera.org/lecture/iot-architecture/device-drivers-AL7YG

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M.Tech. I Year II Semester **Course Structure**

L	T	P	C
3	0	0	3

Low Power VLSI Design

(Professional Elective IV)

INTERNAL MARKS: 40

Course Code: PP21ECE10 **EXTERNAL MARKS: 60**

Course Prerrquisite: VLSI

Course Outcomes:

At the end of the course, students will be able to:

- Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
- Characterize and model power consumption & understand the basic analysis methods.
- Understand leakage sources and reduction techniques

Unit 1:

Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree Of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd& Vt on speed, constraints on Vt reduction, transistor sizing& optimal gate oxide thickness, impact of technology scaling, technology innovations.

Unit 2:

Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

Unit 3:

Low Power Clock Distribution: Power dissipation in clock distribution, single driver Versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. Tolerable skew, chip & package co-design of clock network.

Unit 4:

Logic Synthesis for Low Power estimation techniques: Power minimization techniques, Low power arithmetic components- circuit design styles, adders, multipliers.

Unit 5:

Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits. Low Power Microprocessor Design System: power management support, architectural

trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power.

Text Books:

1. P. Rashinkar, Paterson and L. Singh, “Low Power Design Methodologies”, Kluwer Academic, 2002
2. Kaushik Roy, Sharat Prasad, “Low power CMOS VLSI circuit design”, John Wiley sons Inc.,2000.

Reference Books:

1. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley, 1999.
2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”,Kluwer,1995
3. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

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M.Tech. I Year II Semester **Course Structure**

L	T	P	C
3	3	0	3

TESTING AND TESTABLITY

(Professional Elective-IV)

Internal Marks: 40

Course Code: PP21ECE11 **External Marks: 60**

Course Prerequisite: Digital Circuits

Course Objectives:

1. To understand different fault models and fault simulation techniques.
2. To understand automatic TG (ATG) for SSFs of Combinational and Sequentialcircuits.
3. To understand different testability techniques and compression techniques.
4. To understand build in self test (BIST) process, generation and delay fault.
5. To understand System Configuration with Boundary Scan and Boundary ScanDescription Language.

Course Outcomes:

After successful completion of the course student will be able to

1. Simulate different simulation techniques.
2. Analyze ATG for SSFs of Combinational and Sequential circuits.
3. Develop different testability techniques and compression techniques.
4. Analyze build in self test (BIST) process, generation and delay fault.
5. Implement System Configuration with Boundary Scan and Boundary ScanDescription Language.

UNIT-I **(10 Lectures)**

Fault Modeling:

Logical Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, Single and Multiple Stuck-Fault Model.

Fault Simulation:

General Fault Simulation Techniques, Fault Simulation for Combinational Circuits, Fault Sampling.

UNIT-II **(10 Lectures)**

Testing For Single Stuck Faults:

ATG for SSFs in combinational circuits- fault oriented ATG, Fault independent ATG, Random test generation, ATG for SSFs in sequential circuits- TG using iterative array models, Simulation based TG.

UNIT-III **(11 Lectures)**

Design For Testability:

Testability, Adhoc Design for Testability Techniques, Controllability and Observability by Means of Scan Registers, Generic Scan Based Design**.**

Compression Techniques - General Aspects of Compression Techniques, Ones- Count Compression, Transition-Count Compression, Parity-Check Compression, Syndrome Testing, Signature Analysis.

UNIT-IV **(8 Lectures)**

Built-In Self-Test

The Economic Case for BIST, Random Logic BIST, Memory BIST.

UNIT-V **(9 Lectures)**

Boundary Scan Standard

Motivation, System Configuration with Boundary Scan, Boundary Scan DescriptionLanguage.

Text Books:

1. M. Abramovici, M.A. Breuer and A.D. Friedman (1996), “Digital Systems and Testable Design", Jaico Publishing House.

Reference Books:

1. M.L. Bushnell and V.D. Agrawal (2002), "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwar AcademicPublishers.

Web References:

1. http://www.pld.ttu.ee/diagnostika/theory/fault.html
2. https://www.ida.liu.se/~zebpe83/teaching/test/lec3.pdf
3. https://www.ida.liu.se/~zebpe83/teaching/test/lec4.pdf
4. https://www.ida.liu.se/~TDTS01/lectures/13/lec9.pdf
5. http://courses.ece.ubc.ca/578/notes5.pdf
6. http://www.cad.t.u-tokyo.ac.jp/~timcheng/NOTES/08_bist_2pp.pdf

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M.Tech. I Year II Semester **Course Structure**

L	T	P	C
3	0	0	3

SoC Design
(Professional Elective IV)

Internal Maks: 40

Course Code: PP21ECE12 **External Marks: 60**

Course Prerquisite: VLSI

Course Outcomes:

At the end of the course, students will be able to:
- Identify and formulate a given problem in the framework of SoC based design approaches Design
SoC based system for engineering applications
- Realize impact of SoC on electronic design philosophy and Macro-electronics thereby
- incline towards entrepreneurship & skill development.

Unit 1:

ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

Unit 2:

NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

Unit 3:

Simulation: Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

Unit 4:

Low power SoC design / Digital system: Design synergy, Low power system perspective - power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

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Unit 5 :

Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

Text Books:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006

Reference Books:

1. Rochit Rajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center,2000
2. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008
3. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley

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M.Tech. I Year II Semester **Course Structure**

L	T	P	C
0	0	3	2

CMOS Analog and Digital IC Design Lab

Internal Marks: 40

Course Code: PP21ECL02 **External Marks: 60**

Course Prerequisite: VLSI

- The students are required to design and implement the Circuit and Layout of any **TEN** Experiments using CMOS 130nm Technology with Mentor Graphics Tool/Cadence / Synopsys / Industry Equivalent Standard Software.

List of Experiments:

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. simple current mirror
6. cascode current mirror.
7. Wilson current mirror.
8. Full Adder
9. RS-Latch
10. Clock Divider
11. JK-Flip Flop
12. Synchronous Counter
13. Asynchronous Counter
14. Static RAM Cell

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M.Tech. I Year II Semester **Course Structure**

L	T	P	C
0	0	3	2

Real Time Operating Systems Lab

Internal Marks: 40

Course Code: PP21ECL04 **External Marks: 60**

Course Prerequisite: E.S

- The Students are required to write the programs using C-Language according to the Experiment

requirements using RTOS Library Functions and macros ARM-926 developer kits and ARMCortex.

- The following experiments are required to develop the algorithms, flow diagrams, source code and perform the compilation, execution and implement the same using necessary hardware kits for verification. The programs developed for the implementation should be at the level of an embedded system design.
- The students are required to perform at least SIX experiments from Part-I and TWO experiments from Part-II.

List of Experiments:

Part-I: Experiments using ARM-926 with PERFECT RTOS

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER‟S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader‟s Writer‟s Problem for concurrent Tasks.

Part-II: Experiments on ARM-CORTEX processor using any open source RTOS. (Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Simulate the temperature DATA Logger with the SERIAL communication with PC.
4. Implement the developer board as a modem for data communication using serial port communication between two PC‟s.

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Lab Requirements:

Software:

- Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.
- LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

Hardware:

- The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.
- Serial Cables, Network Cables and recommended power supply for the board

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M.Tech. I Year II Semester **Course Structure**

L	T	P	C
2	0	0	0

CONSTITUTION OF INDIA
(Audit-II)

Internal Marks:

Course Code: PP21ECA02 **External Marks:**

Course Prerequisite:

Course Objectives:

Students will be able to:
1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opinion regarding modern Indian intellectuals‟ constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Course Outcomes:

Students will be able to:
1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival
of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that
informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under
the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

UNIT 1

History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working)

UNIT 2

Philosophy of the Indian Constitution: Preamble Salient Features

UNIT 3

Contours of Constitutional Rights & Duties: Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational

Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT 4.

Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive President, Governor,Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications Powers and Functions.

UNIT 5.

Local Administration: District‟s Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CE of Municipal Corporation. Pachayati raj: Introduction, PRI: ZilaPachayat. Elected officials and their roles, CEO ZilaPachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy

UNIT 6.

Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

Suggested reading

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

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M.Tech. II Year I Semester **Course Structure**

L	T	P	C
3	0	0	3

ARTIFICIAL INTELLIGENCE

(Professional Elective –V)

Internal Marks: 40

Course Code: PP21ECE13 **External Marks: 60**

Course Prerequisite: Mathematics

Course Objectives:

1. To understand artificial intelligence with various models.
2. To understand supervised learning models.
3. To understand unsupervised learning models.
4. To understand the level for randomness in fuzzy sets.
5. To analyse unconstrained optimization techniques.

Course Outcome:

1. Apply artificial intelligence techniques to solve engineering problem.
2. Handling supervised learning with proper training set.
3. Handling unsupervised learning without training set.
4. Creating membership functions for quantifying the amount of randomness.
5. Incorporating unconstrained optimization in to solve engineering problems.

UNIT-1 **(9 Lectures)**

Introduction to Artificial Neural Networks: Fundamental concepts: Artificial neural networks, Biological neural networks, Brain versus computer, Basic model of artificial neural network, Important Technologies of artificial neural network, McCulloch-Pitts Model.

UNIT-II **(10 Lectures)**

A Survey of Neural Network Models: supervised learning : Perception model, ADALINE (Adaptive Linear neuron)-algorithm : Theory, Architecture, Flowchart of training process, Training algorithm, Testing algorithm, Multiple Adaptive Linear neuron MADALINE-algorithm Theory, Architecture, Flowchart of training process, Training algorithm, Testing algorithm. Back propagation networks Theory, Architecture, Flowchart of training process, Learning factors of Back propagation networks, Testing algorithm of Back propagation networks.

UNIT-III **(10 Lectures)**

A Survey of Neural Network Models: unsupervised learning: Kohonen Self organizing Feature map: Theory, Architecture, Flowchart, Training Algorithm, Kohonen Self organizing map. Learning Vector Quantization: Theory, Architecture, Flowchart, Training Algorithm, Variants. Counter propagation networks: Theory, Full counter propagation Net, Forward only counter propagation Net. Adaptive Resonance theory.

UNIT-IV **(10 Lectures)**

Fuzzy sets Classical Sets : Operations on Classical Sets, Properties of Classical (Crisp) Sets, Mapping of Classical Sets. Fuzzy Sets Fuzzy Set Operations, Properties of Fuzzy Sets, Alternative Fuzzy Set Operation. Properties of Membership Functions, Fuzzification, and Defuzzification Features of the Membership Function, Various Forms, Fuzzification, Defuzzification to Crisp Sets, λ-Cuts for Fuzzy Relations, Defuzzification to Scalars.

UNIT-V **(9 Lectures)**

Optimization Techniques Unconstrained Optimization: Basics of set constrained and unconstrained optimization. One dimensional search methods. Gradient method, Newton method, Conjugate direction methods, Quasi newton methods. Global search algorithms: Simulated annealing, Particle swarm optimization and Genetic algorithm.

Textbooks:

1. Principles of Soft Computing by S. N. Sivanandam, S. N. Deepa, Wiley-India.
2. Neural Networks Fuzzy Logic & Genetic Alogrithms by Rajshekaran & Pai,Prentice Hall.

References :

1. Fuzzy Logic with Engineering Applications., McGraw Hill,Second edition RossT.J.,
2. An Introduction to Optimization Edwin K., P. Chong & Stanislaw h. Zak

Web Reference :

1.http://vlabs.iitkgp.ernet.in/scte/
2. http://cse22-iiith.vlabs.ac.in/
3. https://swayam.gov.in/course/4574-introduction-to-soft-computing.
4. https://www.hindawi.com/journals/mpe/soft.computing/
5. https://in.mathworks.com/products/optimization.html?requestedDomain

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M.Tech. II Year I Semester

Course Structure

L	T	P	C
3	0	0	3

ASIC DESIGN

(Professional Elective -V)

Internal Marks: 40

Course Code: PP21ECE14 **External Marks: 60**

Course Prerequisite: Basics of VLSI,STLD

Course Objectives:

1. To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
2. To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.
3. To gain a knowledge on low level design entry and synthesis for ASIC‘s.
4. To gain knowledge on simulation, partitioning and testing of ASIC’s.
5. To give the student an understanding of placement , routing techniques

Course Outcomes:

On successful completion of this course the students will be able to

1. Student can demonstrate in-depth knowledge in ASIC Design Styles, ASICs Design issues, ASICs Design Techniques, ASIC Construction.
2. Student can analyze the characteristics and Performance of ASICs and judge independently the best suited device for fabrication of smart devices for conducting research in ASIC design.
3. Student is able to give the design entry of devices using HDL’s and able to synthesis them.
4. Student can solve problems of Design issues, simulation and Testing of ASICs.
5. Student can apply appropriate techniques, resources and tools to engineering activities for appropriate Solution to develop ASICs.

UNIT-I **(10 Lectures)**

Introduction to ASICs:

Types of ASICs- Full-Custom ASICs, Semicustom ASICs, Standard cell based ASICs, Gate-array based ASICs, Channeled Gate Array, Channel less Gate Array, Structured Gate Array, Programmable Logic Devices, Field-Programmable Gate Arrays, ASIC Design Flow. **MASTER OF TECHNOLOGY(VLSI&ES)** 39

UNIT-II **(9 Lectures)**

ASIC Library Design & Programmable ASICs: ASIC Cell Libraries, , Library cell design, Library Architecture, Gate-Array Design, Standard-Cell Design, Data path-Cell Design. Transistors as Resistors, Transistor Parasitic Capacitance **Programmable ASICS:** Anti fuse, Static RAM, EPROM and EEPROM technology.

UNIT-III **(10 Lectures)**

Low-Level Design Entry & Logic Synthesis: Schematic Entry, Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, Vectored instances and Buses, Edit-in-place, Attributes, Net list Screener, Back-Annotation, logic-Synthesis**,** Verilog and Logic Synthesis, VHDL and Logic Synthesis

UNIT-IV **(11 Lectures)**

Simulation, Testing & ASIC Construction: Types of Simulation -Structural Simulation, Gate-Level Simulation, Static Timing Analysis, Formal Verification, Switch-Level Simulation, Transistor-Level Simulation, Boundary Scan Test, Faults, Fault simulation, Automatic Test-Pattern Generation

ASIC Construction: Physical Design, System Partitioning, FPGA Partitioning, Partitioning Methods.

UNIT-V **(8 Lectures)**

Floor Planning, Placement & Routing:

Floor planning, Placement, Physical Design Flow, Global Routing, Detailed Routing, Special Routing, Circuit Extraction and DRC.

Text Books:

1. M.J.S .Smith, - "Application - Specific Integrated Circuits" – Pearson Education, 2003.

Reference Books:

1. Jose E.France, Yannis Tsividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing", Prentice Hall, 1994.

Website Reference:

1. https://www.radio-electronics.com › Electronic components
2. www.sigenics.com/blog/
3. vlsibyjim.blogspot.com/2015/03/floorplanning.html
4. https://electronics.stackexchange.com/questions/.../floorplanning-vs-placement-in-vlsi

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M.Tech. II Year I Semester

Course Structure

L	T	P	C
3	0	0	3

PARALLEL PROCESSING

(Elective V)

Internal Marks: 40

Course Code: PP21ECE15 **External Marks: 60**

Course Prerequisite: Mathematics

Course Outcomes:

At the end of this course, students will be able to

- Identify limitations of different architectures of computer
- Analysis quantitatively the performance parameters for different architectures
- Investigate issues related to compilers and instruction set based on type of architectures.

Unit 1:

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability

Unit 2:

Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

Unit 3:

VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC,MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

Unit 4:

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions

Unit 5:

Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Operating systems for multiprocessors systems Customizing applications on parallel processing platforms

Text Books:

1. Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing”, MGH International Edition
2. Kai Hwang, “Advanced Computer Architecture”, TMH
3. V. Rajaraman, L. Sivaram Murthy, “Parallel Computers”, PHI.

Reference Books:

1. William Stallings, “Computer Organization and Architecture, Designing for performance “Prentice Hall, Sixth edition
2. Kai Hwang, ZhiweiXu, “Scalable Parallel Computing”, MGH
3. David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan

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M.Tech.II Year I Semester **Course Structure**

L	T	P	C
3	0	0	3

INDUSTRIAL SAFETY
(Open Elective)

Internal Marks: 40

Course Code: PP21ECO01 **External Marks: 60**

Course Prerequisite: Mathematics

Unit-1:

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, quipment and methods.

Unit-2:

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

Unit-3:

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i.Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v.Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

Unit-4:

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment"s like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine,v. Boiler,vi .Electrical motors, Types of faults in machine tools and their general causes.

Unit-5:

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii.Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and

electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Reference:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da InformationServices.
2. Maintenance Engineering, H. P. Garg, S. Chand andCompany.
3. Pump-hydraulic Compressors, Audels, McgrewHillPublication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman &HallLondon

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M.Tech. II Year I Semester

Course Structure

L	T	P	C
3	0	0	3

OPERATIONS RESEARCH
(Open Elective)

Internal Marks: 40

Course Code: PP21ECO02 **External Marks: 60**

Course Prerequisite: Mathematics

Course Outcomes:

At the end of the course, the student should be able to
1. Students should able to apply the dynamic programming to solve problems of discreet and continuous variables.
2. Students should able to apply the concept of non-linear programming
3. Students should able to carry out sensitivity analysis
4. Student should able to model the real world problem and simulate it.

Unit 1:

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models

Unit 2

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming

Unit 3:

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem- CPM/PERT

Unit 4

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Unit 5

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

References:

1. H.A. Taha, Operations Research, An Introduction, PHI, 2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008
4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009
5. Pannerselvam, Operations Research: Prentice Hall of India 2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010

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M.Tech.II Year I Semester **Course Structure**

L	T	P	C
3	0	0	3

COST MANAGEMENT OF ENGINEERING PROJECTS
(Open Elective)

Internal Marks: 40

Course Code: PP21ECO03 **External Marks: 60**

Course Prerequisite: Mathematics

Introduction and Overview of the Strategic Cost Management Process
Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.
Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control.

Bar charts and Network diagram. Project commissioning: mechanical and process
Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing. Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

References:

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi
2. Charles T. Horngren and George Foster, Advanced Management Accounting
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.